Power Quality Enhancement Using a Z-Source Inverter-Based Dynamic Voltage Restorer With PLL-Synchronized PI Control

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Abstract
Voltage sag, voltage swell, and supply interruptions constitute nearly 80% of power quality disturbances in modern distribution networks, causing significant global economic losses due to equipment malfunction and production downtime. Mitigating these disturbances is critical for sensitive infrastructures such as semiconductor fabrication plants, data centers, and medical facilities. However, conventional Dynamic Voltage Restorer (DVR) systems exhibit limited compensation capability during unbalanced faults, sluggish dynamic responses, and elevated harmonic injection. To overcome these limitations, this paper presents a Z-Source Inverter-based Dynamic Voltage Restorer (ZSI-DVR) integrated with a Phase-Locked Loop (PLL) synchronized Proportional-Integral (PI) control strategy. The architecture leverages a symmetric Z-source impedance network to provide inherent single-stage voltage boost capability, eliminating the need for bulky front-end DC–DC converters. The PLL ensures precise grid synchronization, while the PI controller regulates the series injection transformer to dynamically counteract voltage anomalies. Simulation and experimental validations demonstrate that the proposed ZSI-DVR drastically improves voltage restoration accuracy, accelerates transient response, and enhances load-side power quality and reliability under volatile grid conditions.

Keywords: Dynamic Voltage Restorer (DVR), Z-source inverter (ZSI), phase-locked loop (PLL), proportional–integral (PI) controller, power quality, voltage sag, voltage swell.

1. Introduction

Power quality has emerged as one of the most significant concerns in modern electrical power systems due to the widespread deployment of sensitive electronic equipment, automated manufacturing facilities, data centres, healthcare infrastructure, and digital communication networks. According to several industrial power quality surveys, voltage sag events account for nearly 80% of all power quality disturbances experienced in distribution networks. Studies conducted by international utility organizations indicate that industrial facilities experience multiple voltage disturbances annually, leading to equipment malfunction, production losses, and increased maintenance costs. The increasing integration of renewable energy resources, electric vehicle charging stations, nonlinear loads, and distributed generation units has further intensified voltage fluctuations within power distribution systems. As a result, maintaining voltage stability and ensuring uninterrupted power delivery have become critical requirements for modern utility operators and industrial consumers.

Figure 1 illustrates the classification of custom power devices used in modern power distribution systems to enhance power quality and improve system reliability. Custom power devices are specialized power electronic equipment designed to mitigate disturbances such as voltage sag, voltage swell, harmonics, interruptions, flicker, and transient events. As shown in the figure, these devices are broadly categorized into two major groups: Network Reconfiguration Type and Compensating Type devices. Network reconfiguration devices primarily focus on modifying the network configuration to protect loads and improve fault tolerance, whereas compensating devices directly inject or absorb voltage and current components to maintain power quality at the load side.

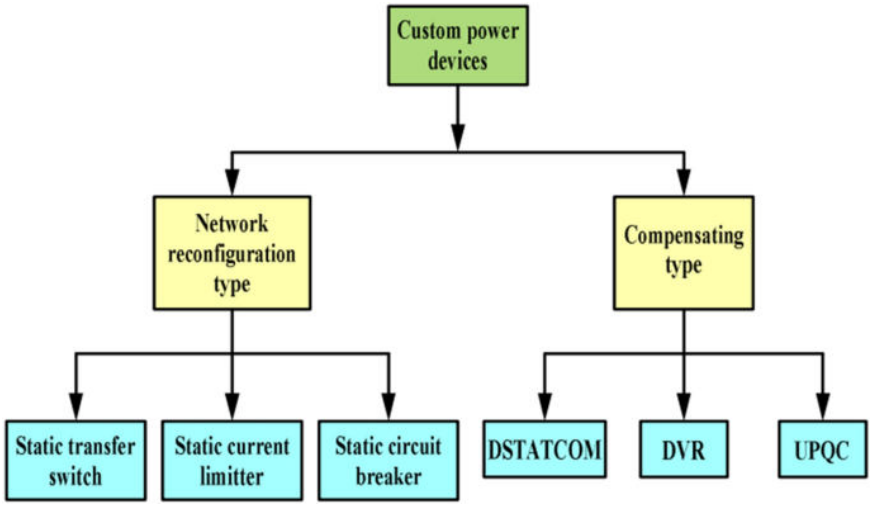

Figure. 1. Classification of custom power devices for power quality improvement.

Table 1. Advantages of DVR over other custom power devices

Feature	DVR	DSTATCOM	UPQC	Static Transfer Switch
Voltage Sag Compensation	Excellent	Moderate	Excellent	Limited
Voltage Swell Compensation	Excellent	Moderate	Excellent	Poor
Interruption Compensation	Excellent	Limited	Excellent	Limited
Voltage Regulation	Excellent	Good	Excellent	Poor
Current Compensation	No	Yes	Yes	No
Harmonic Compensation	Limited	Good	Excellent	No
Cost	Moderate	Moderate	High	Low
Response Speed	Very Fast	Fast	Fast	Moderate
Installation Complexity	Moderate	Moderate	High	Low
Protection of Sensitive Loads	Excellent	Good	Excellent	Limited

The Network Reconfiguration Type includes Static Transfer Switch (STS), Static Current Limiter (SCL), and Static Circuit Breaker (SCB), which are mainly used for fault isolation, current limiting, and rapid transfer of loads between feeders during abnormal conditions. The Compensating Type consists of Distribution Static Synchronous Compensator (DSTATCOM), Dynamic Voltage Restorer (DVR), and Unified Power Quality Conditioner (UPQC). DSTATCOM is primarily employed for reactive power compensation and voltage regulation, DVR is widely used for mitigating voltage sag, voltage swell, and interruption disturbances through series voltage injection, and UPQC combines both series and shunt compensation capabilities to address voltage and current quality problems simultaneously, as shown in table 1. These custom power devices play a significant role in improving power quality, enhancing system stability, and ensuring reliable operation of sensitive industrial, commercial, and residential loads.

2. Literature Survey

A. Grid-Level Voltage Sag Characterization and Emulation

The increasing penetration of renewable energy resources, such as wind and solar photovoltaic systems, leaves power networks highly susceptible to grid-fault-induced voltage disturbances. Han *et al.* [1] conducted a comprehensive review of voltage sag characteristics and generation techniques used to evaluate the Low-Voltage Ride-Through (LVRT) capability of renewable energy configurations. The authors categorized sags caused by short-circuit faults, transformer energization, and heavy motor

starting based on severity, duration, and fault profiles. They systematically compared generator-based, shunt impedance-based, transformer-based, and full converter-based sag generators, noting that full converter-based architectures provide superior flexibility and emulation precision. Their framework was further validated using a Real-Time Digital Simulator (RTDS) hardware-in-the-loop (HIL) setup to analyze the LVRT capabilities of permanent magnet synchronous generator (PMSG) wind turbines.

B. Advanced Dynamic Voltage Restorer (DVR) Topologies and Direct AC/AC Converters

To protect sensitive local loads from grid sags, swells, and short-duration interruptions, various Dynamic Voltage Restorer (DVR) structures have been engineered to balance compensation capability against circuit complexity. Traditional DVR designs often depend on heavy energy storage blocks or complex conversion topologies. To lower hardware requirements, Abuthahir *et al.* [7] proposed a compact, energy-storage-free DVR topology utilizing a direct AC/AC converter with only three bidirectional switches. Connected between the utility grid and a center-tapped series transformer, this configuration extracts power directly from the supply line to mitigate up to 50% voltage sags and unlimited voltage swells while cutting switching losses. This hardware-reduction approach was also explored by Rahman *et al.* [13], who designed a three-phase direct converter-based DVR using only three bidirectional switches per phase paired with a multi-winding transformer layout. Similarly, Rahman *et al.* [3] validated a simplified single-phase matrix converter architecture that trims the typical eight-switch requirement down to four controlled switches, maintaining bidirectional AC-to-DC and DC-to-AC power conversion with a simplified gate-pulse routine.

To maximize voltage restoring ranges without cascading multi-stage inverters, multi-winding transformer arrangements have been widely adopted. Rahman *et al.* [6] developed an enhanced DVR topology that mixes multiple three-phase voltage sources at the converter input via a multi-winding transformer configuration. This layout achieved an extended compensation span, mitigating voltage sags up to 68% and absorbing voltage swells up to 500% while maintaining a total harmonic distortion (THD) below 5%. For environments where active power components must be eliminated entirely to maximize system reliability, Rahman *et al.* [14] developed a converter-free voltage disturbance compensator. This architecture completely removes power electronic converters, pulse-width modulation (PWM) modules, controllers, and harmonic filters. Operating via a multi-winding transformer, a voltage-controlled voltage source, and two bidirectional switches per phase, the device draws compensation energy directly from healthy grid phases, providing long-duration mitigation at a low installation cost.

C. Control Algorithms, Synchronization, and Energy Storage Integration

Beyond hardware topology, the dynamic performance of a DVR depends heavily on its synchronization and control loop design. To bypass the processing overhead of modern digital controllers, Rahman *et al.* [10] developed a carrier-based PWM control framework integrated with an analog feed-forward control structure for a three-phase DVR. This architecture eliminates complex phase-to-phase calculation loops by drawing compensation power from healthy phases or the disturbed line itself to restore nominal load voltage. Alternative hardware-driven control configurations include the battery-supported DVR developed by Rahman *et al.* [2] and Rahman and Somasundaram [12]. Placed at the output side of a distribution transformer, these designs utilize dedicated battery energy storage systems (BESS), filtering blocks, and a series injection transformer to monitor and regulate terminal voltage without relying on traditional proportional-integral (PI), fuzzy logic, or neural network algorithms.

Conversely, when highly responsive analytical tracking is required, Synchronous Reference Frame (SRF) theory is often employed. Rahman and Somasundaram [9] developed a storage-free DVR combining SRF sequence extraction with a hysteresis current controller and a phase-locked loop (PLL) to inject accurate compensating vectors through a voltage source inverter (VSI). To optimize voltage boosting and minimize passive filter component sizes, Moghassemi *et al.* [11] replaced the standard VSI with a Trans-Z-Source Inverter (TransZSI). They integrated a Unit Vector Template (UVT)

detection method with a Maximum Constant Boost Control (MCBC) switching scheme. This hybrid UVT-MCBC approach expands the voltage buck-boost range, lowers semiconductor voltage stress, and reduces harmonic distortion in the injected series voltage. For hybrid PV-wind distributed networks, Molla and Kuo [15] introduced a DVR backed by a combined BESS and Superconducting Magnetic Energy Storage (SMES) unit. Their control design uses a pre-sag compensation strategy that continuously records voltage magnitudes and phase angles at the Point of Common Coupling (PCC) during normal operation. During grid faults, the recorded baseline vectors are immediately deployed to restore balance under both symmetrical and asymmetrical voltage sags.

D. Industrial Harmonic Filtering and Delayed Network Stability

Auxiliary power quality challenges, particularly harmonic distortion from nonlinear loads, require targeted line filtering. The authors in [4] performed a comparative performance assessment of industrial harmonic filtering techniques utilizing the National Tobacco Enterprise of Ethiopia as a practical case study. They evaluated single-tuned, double-tuned, high-pass, and C-type filters under identical load conditions. Their results demonstrated that while all configurations suppressed line harmonics, the double-tuned harmonic filter delivered the lowest current and voltage THD, proving to be the most reliable option for industrial harmonic mitigation.

In parallel with physical filtering, maintaining the theoretical stability of automated grid control loops requires mathematical verification against networking delays. Tan and Wang [5] proposed a stability analysis framework for recurrent neural networks subject to time-varying delays. By introducing a Flexible Negative-Determination Quadratic Function (FNDQF) paired with enhanced integral inequalities and Lyapunov–Krasovskii functionals, they established a set of Linear Matrix Inequalities (LMIs) that reduce analytical conservatism. This mathematical bounding was expanded by Hu *et al.* [8], who addressed the H_∞ state estimation problem in delayed neural networks. They introduced an extended reciprocally convex inequality using an r-degree polynomial matrix inequality. This mathematical integration yields tighter bounds for Lyapunov–Krasovskii derivatives, allowing exact derivation of optimal estimator gains and improving state tracking accuracy in delayed systems.

3. Proposed System

To overcome the limitations associated with conventional voltage compensation systems, a more efficient and reliable solution is required that can provide rapid voltage restoration, enhanced disturbance mitigation capability, improved voltage regulation accuracy, and stable operation under varying grid conditions. The proposed system is designed to maintain high-quality power supply during voltage sag, voltage swell, and interruption events while improving system reliability, reducing harmonic distortion, enhancing energy utilization efficiency, and ensuring uninterrupted operation of sensitive loads. Such an advanced compensation framework is essential for modern smart grids, industrial facilities, healthcare systems, data centers, and other critical applications where continuous and stable power delivery is mandatory. Figure 2 illustrates the proposed ZSI-DVR integrated with a PI controller for mitigating voltage sag, voltage swell, and interruption disturbances in a three-phase distribution system. The proposed system consists of a three-phase grid source, distribution transformer, Z-Source Network, VSI, LC output filter, series injection transformers, breakers, and a PI-based control system. Unlike conventional DVR structures, the proposed configuration employs a Z-Source Network between the DC source and inverter, enabling both buck and boost voltage conversion capabilities through shoot-through operation. The PI controller continuously regulates the injected voltage by comparing the load voltage with the reference voltage in the synchronous dq reference frame, thereby ensuring effective compensation and maintaining the load voltage at its rated value during various power quality disturbances.

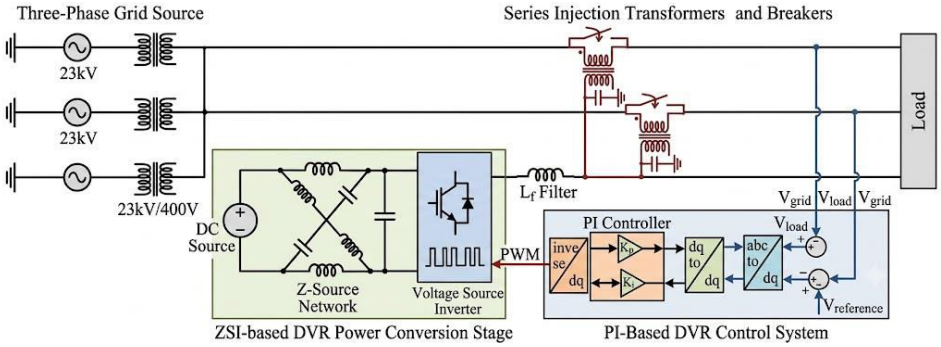

Figure 2. Topology of the proposed ZZSI-DVR with PI controller.

Three-Phase Grid Source and Distribution Transformer: The three-phase utility grid supplies electrical power at 23 kV. The distribution transformer reduces the voltage level from 23 kV to 400 V for distribution to low-voltage loads. Under normal operating conditions, the source voltage is directly supplied to the load. The supply voltage is continuously monitored for the occurrence of voltage sag, voltage swell, or interruption conditions. The three-phase source voltage is represented as

$$V_{grid} = [V_a \; V_b \; V_c \;] \tag{3.1}$$

where V_a, V_b, and $V_c$are the phase voltages of the three-phase system.

DC Source and Energy Supply: A DC energy source supplies power to the Z-Source Inverter. The DC source provides the necessary energy required for voltage compensation during power quality disturbances. During voltage sag and interruption conditions, the stored DC energy is utilized by the inverter to generate the required compensating voltage. The DC source voltage is represented as V_{dc}, where V_{dc}denotes the input DC voltage supplied to the Z-source network.

Z-Source Network Operation: The Z-Source Network consists of two inductors $(L_2)$and two capacitors (C_2)connected in an X-shaped impedance configuration. This network provides unique buck–boost capability that is not available in conventional voltage source inverters. The capacitor voltage boost factor is expressed as

$$B = \frac{1}{1-2D_{ST}} \tag{3.2}$$

were

- B= Boost factor
- D_{ST}= Shoot-through duty ratio

The boosted DC-link voltage becomes

$$V_{boost} = BV_{dc} \tag{3.3}$$

where $V_{boost}$is the enhanced DC-link voltage applied to the inverter. The Z-source network allows the inverter to generate compensation voltages greater than the available DC source voltage without requiring an additional DC–DC converter.

Voltage Source Inverter (VSI): The Voltage Source Inverter converts the boosted DC voltage into controlled three-phase AC voltages. The inverter switching devices operate according to PWM signals generated by the control system. The inverter output voltage is given by

$$V_{inv} = MBV_{dc} \tag{3.4}$$

were

- V_{inv}= Inverter output voltage
- M= Modulation index
- B= Boost factor
- V_{dc}= Input DC voltage

This capability enables effective voltage injection even under severe sag conditions.

LC Output Filter: The inverter output contains switching harmonics generated during PWM operation. Therefore, an LC filter consisting of filter inductance L_f and filter capacitance C_f is connected at the inverter output. The filter resonant frequency is

$$f_r = \frac{1}{2\pi\sqrt{L_f C_f}} \quad (3.5)$$

were

- L_f= Filter inductance
- C_f= Filter capacitance
- f_r= Resonant frequency

The filter removes high-frequency harmonics and produces a smooth sinusoidal compensating voltage.

Measurement of Grid and Load Voltages: The controller continuously measures both the grid voltage and load voltage. The voltage error signal is determined as

$$e(t) = V_{reference} - V_{load} \quad (3.6)$$

were

- $e(t)$= Voltage error
- $V_{reference}$= Desired rated voltage
- V_{load}= Measured load voltage

The generated error indicates the amount of compensation required.

abc-to-dq Transformation: The measured three-phase voltages are transformed into the synchronous rotating dq reference frame for simplified control.

$$\begin{bmatrix} V_d \; V_q \end{bmatrix} = \frac{2}{3}\begin{bmatrix} cos\ cos\ \theta & cos\ (\theta - \frac{2\pi}{3}) & cos\ (\theta + \frac{2\pi}{3}) \\ -sin\ \theta & -sin\ (\theta - \frac{2\pi}{3}) & -sin\ (\theta + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} V_a \; V_b \; V_c \end{bmatrix} \quad (3.7)$$

were

- V_d= Direct-axis voltage
- V_q= Quadrature-axis voltage
- θ= Synchronous reference frame angle

The dq transformation converts sinusoidal quantities into DC quantities under balanced conditions, simplifying controller design.

PI Controller Operation: The PI controller processes the voltage error and generates an appropriate control signal for compensation. The PI controller transfer function is

$$G_{PI}(s) = K_p + \frac{K_i}{s} \quad (3.8)$$

were

- K_p= Proportional gain
- K_i= Integral gain

The controller output is expressed as

$$u(t) = K_p e(t) + K_i \int e(t)\, dt \quad (3.9)$$

were

- $u(t)$= Controller output
- $e(t)$= Voltage error signal

The proportional component provides rapid response, while the integral component eliminates steady-state error and improves voltage regulation accuracy.

dq-to-abc Transformation: The compensating voltage generated by the PI controller in the dq frame is converted back into three-phase quantities through inverse Park transformation.

$$[V_{ca}\, V_{cb}\, V_{cc}\,] = \left[cos\ cos\ \theta \quad -sin\ \theta\ cos\ (\theta - \frac{2\pi}{3}) \quad -sin\ (\theta - \frac{2\pi}{3})\ cos\ (\theta + \frac{2\pi}{3}) \quad -sin\ (\theta + \frac{2\pi}{3})\right] [V_d^*\, V_q^*\,] \tag{3.10}$$

were

- V_d^*, V_q^*= Reference compensation voltages
- V_{ca}, V_{cb}, V_{cc}= Three-phase compensation voltages

These voltages serve as references for PWM generation.

PWM Pulse Generation: The reference compensation voltages are applied to the PWM block to generate switching pulses for the inverter. The modulation index is

$$M = \frac{V_{ref}}{V_{carrier}} \tag{3.11}$$

were

- M= Modulation index
- V_{ref}= Reference voltage
- $V_{carrier}$= Carrier waveform amplitude

The generated PWM signals control the inverter switches and determine the injected voltage magnitude.

Series Injection Transformer and Voltage Compensation: The inverter-generated compensating voltage is injected into the distribution feeder through the series injection transformers. The injected voltage compensates for the difference between the source voltage and the desired load voltage. The load voltage is given by

$$V_{load} = V_{grid} + V_{inj} \tag{3.12}$$

were

- V_{load}= Load voltage
- V_{grid}= Grid voltage
- V_{inj}= Injected DVR voltage

For voltage sag compensation, $V_{inj}$is injected in phase with the source voltage. For voltage swell compensation, the injected voltage opposes the source voltage.

Load Voltage Restoration: After compensation, the load voltage remains balanced and maintained at its rated magnitude despite grid disturbances. The combination of the Z-Source Inverter and PI controller enables higher voltage boosting capability, improved compensation range, reduced converter stress, enhanced reliability, and superior power quality performance compared with conventional DVR topologies. The proposed ZSI-DVR effectively mitigates balanced and unbalanced voltage sags, voltage swells, and supply interruptions while ensuring continuous operation of sensitive loads.

3.1 Proposed Control Circuit for ZSI-DVR

The proposed control circuit shown in Figure 3 employs a DQ0-reference frame-based PI control strategy for the ZSI-DVR. The controller continuously monitors the three-phase source voltages and transforms them into the synchronous rotating DQ0 reference frame using a PLL. Separate PI controllers are utilized for the direct-axis (d), quadrature-axis (q), and zero-sequence (0) components to accurately regulate voltage disturbances. The generated control signals are transformed back into three-phase quantities and used to produce PWM switching pulses for the inverter. This control approach provides fast dynamic response, eliminates steady-state error, improves voltage regulation, and ensures effective compensation of balanced and unbalanced voltage sags, swells, and interruptions.

Three-Phase Voltage Measurement: The three-phase source voltages are continuously measured and represented as

$$V_{sabc} = [V_{sa}\, V_{sb}\, V_{sc}\,] \tag{3.13}$$

where:

- V_{sa}= Phase-A voltage

- V_{sb}= Phase-B voltage
- V_{sc}= Phase-C voltage

These voltages serve as the input signals to the control system and are monitored continuously for disturbance detection.

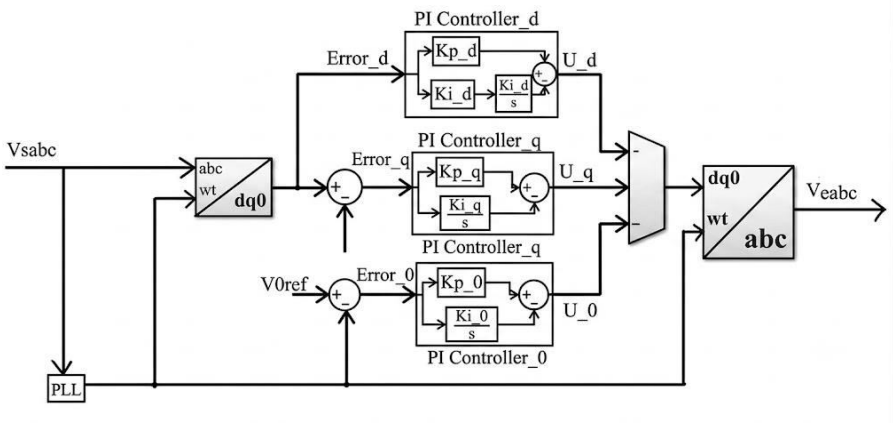

Figure 3. Proposed PI Control Circuit for ZSI-DVR.

PLL Synchronization: A PLL is employed to extract the phase angle of the grid voltage and synchronize the controller with the utility system. The angular position is given by

$$\theta = \omega t \tag{3.14}$$

where:

- θ= Synchronous reference angle
- ω= Angular frequency (rad/s)
- t= Time

The PLL ensures accurate coordinate transformation and proper synchronization between the grid and inverter.

abc-to-dq0 Transformation: The measured three-phase voltages are transformed into the synchronous DQ0 reference frame using Park's transformation.

$$\left[V_d\ V_q\ V_0\ \right] = \frac{2}{3}\left[cos\ cos\ \theta\ \ cos\ (\theta - \frac{2\pi}{3})\ cos\ (\theta + \frac{2\pi}{3})\ \ - sin\ \theta\ \ - sin\ (\theta - \frac{2\pi}{3})\ \ - sin\ (\theta + \frac{2\pi}{3})\ \frac{1}{2}\ \frac{1}{2}\ \frac{1}{2}\right]\left[V_{sa}\ V_{sb}\ V_{sc}\ \right] \tag{3.15}$$

where:

- V_d= Direct-axis voltage component
- V_q= Quadrature-axis voltage component
- V_0= Zero-sequence voltage component

The transformation converts AC quantities into DC quantities under balanced conditions, simplifying controller implementation.

Generation of Reference Voltages: The controller establishes desired reference values corresponding to the rated operating condition.

$$V_{dref} = 1\ pu, V_{qref} = 0, V_{0ref} = 0 \tag{3.16}$$

where:

- V_{dref}= Direct-axis reference voltage
- V_{qref}= Quadrature-axis reference voltage
- V_{0ref}= Zero-sequence reference voltage

These references define the desired load voltage conditions.

Error Signal Generation: The transformed voltage components are compared with their respective reference values to determine compensation requirements. The d-axis error is

$$Error_d = V_{dref} - V_d \quad (3.17)$$

The q-axis error is

$$Error_q = V_{qref} - V_q \quad (3.18)$$

The zero-sequence error is

$$Error_0 = V_{0ref} - V_0 \quad (3.19)$$

where:

- $Error_d$= Direct-axis voltage error
- $Error_q$= Quadrature-axis voltage error
- $Error_0$= Zero-sequence voltage error

These error signals indicate the magnitude of voltage deviation caused by disturbances.

D-Axis PI Controller Operation: The d-axis error signal is processed through the PI controller responsible for regulating the voltage magnitude. The controller output is

$$U_d = K_{p_d} Error_d + K_{i_d} \int Error_d \, dt \quad (3.20)$$

where:

- U_d= d-axis control output
- K_{p_d}= Proportional gain of d-axis controller
- K_{i_d}= Integral gain of d-axis controller

The proportional term provides immediate corrective action, while the integral term eliminates steady-state voltage error.

Q-Axis PI Controller Operation: The q-axis controller regulates phase imbalance and reactive voltage components. The controller output is

$$U_q = K_{p_q} Error_q + K_{i_q} \int Error_q \, dt \quad (3.21)$$

where:

- U_q= q-axis control output
- K_{p_q}= Proportional gain
- K_{i_q}= Integral gain

This controller minimizes phase deviation and improves voltage balance during unbalanced disturbances.

Zero-Sequence PI Controller Operation: The zero-sequence PI controller compensates for neutral and unbalanced fault components. The output is

$$U_0 = K_{p_0} Error_0 + K_{i_0} \int Error_0 \, dt \quad (3.22)$$

where:

- U_0= Zero-sequence control signal
- K_{p_0}= Proportional gain
- K_{i_0}= Integral gain

The controller suppresses zero-sequence voltage components generated during single-phase and unbalanced faults.

Formation of Control Voltage Vector: The outputs of the three PI controllers are combined to form the compensation voltage vector in the DQ0 frame.

$$U_{dq0} = \left[U_d \; U_q \; U_0 \right] \quad (3.23)$$

This vector represents the required compensating voltage that must be generated by the DVR.

dq0-to-abc Inverse Transformation: The compensation voltage vector is converted back into three-phase quantities using inverse Park transformation.

$$[V_{ea}\, V_{eb}\, V_{ec}\,] = \left[cos\ cos\ \theta \quad -sin\ \theta\ 1\ cos\ (\theta - \frac{2\pi}{3}) \quad -sin\ (\theta - \frac{2\pi}{3})\ 1\ cos\ (\theta + \frac{2\pi}{3}) \quad -sin\ (\theta + \frac{2\pi}{3})\ 1\right] [U_d\ U_q\ U_0\,] \qquad (3.24)$$

Where, V_{ea}, V_{eb}, V_{ec}= Three-phase compensation voltage references. These signals are used to generate inverter switching commands.

PWM Signal Generation: The three-phase compensation references are supplied to the PWM generator to create switching pulses for the Z-Source Inverter. The modulation index is given by

$$M = \frac{V_{control}}{V_{carrier}} \qquad (3.25)$$

where:

- M= Modulation index
- $V_{control}$= Controller output voltage
- $V_{carrier}$= Carrier signal amplitude

The PWM pulses control the inverter switches and determine the magnitude of the injected compensation voltage.

Compensating Voltage Injection: The Z-Source Inverter generates the required compensation voltage, which is injected into the distribution feeder through the series transformer. The load voltage becomes

$$V_{load} = V_{grid} + V_{inj} \qquad (3.26)$$

where:

- V_{load}= Restored load voltage
- V_{grid}= Disturbed source voltage
- V_{inj}= DVR injected voltage

The injected voltage compensates for the missing or excess voltage caused by grid disturbances.

Voltage Restoration and Power Quality Improvement: After compensation, the load voltage remains balanced and regulated at its rated value even under severe voltage sag, swell, and interruption conditions. The independent PI regulation of d-axis, q-axis, and zero-sequence components enables precise voltage control, faster transient response, reduced steady-state error, enhanced disturbance rejection capability, and improved power quality performance. Consequently, the proposed DQ0-based PI control strategy significantly enhances the effectiveness of the ZSI-DVR in protecting sensitive loads from power quality disturbances.

4. Results and Discussion

Figure 4 illustrates the proposed Z-Source Inverter based Dynamic Voltage Restorer (ZSI-DVR) configuration employed for voltage disturbance mitigation. Unlike the conventional DVR, the proposed system incorporates a Z-source impedance network consisting of two inductors (L1 and L2) and two capacitors (C1 and C2) positioned between the DC source and the inverter. This unique impedance network provides both voltage buck and boost capabilities without requiring an additional DC–DC converter. The inverter output is connected through a three-phase breaker, RL filter, RC filter, and series injection transformer to the distribution feeder. The Z-source network enhances the voltage boosting capability of the DVR, enabling compensation of deeper voltage sags and severe disturbances while improving system reliability and reducing inverter stress. Figure 5 presents the PI controller-based control structure used in the proposed ZSI-DVR. The measured three-phase voltages are transformed into the dq0 reference frame using PLL synchronization. The direct-axis voltage reference is maintained at 1 p.u., while the quadrature-axis and zero-sequence references are maintained at 0 p.u. The generated voltage errors are processed through PI controllers to improve dynamic response and eliminate steady-state errors. The resulting compensation signals are

transformed back into the abc reference frame and supplied to the PWM generator. This control strategy provides more accurate voltage restoration, faster disturbance response, and improved stability compared to the conventional control scheme.

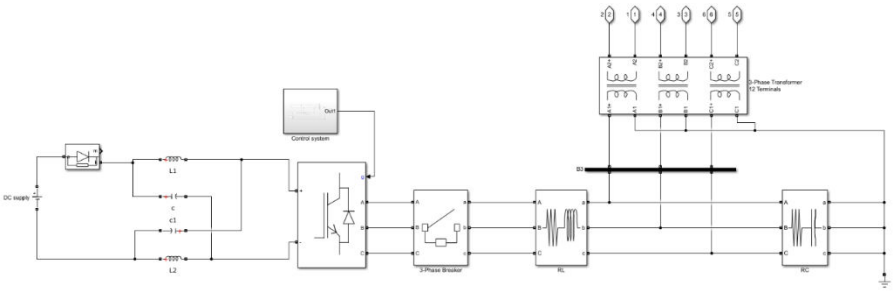

Figure 4. Proposed ZSI-DVR power circuit with Z-Source network.

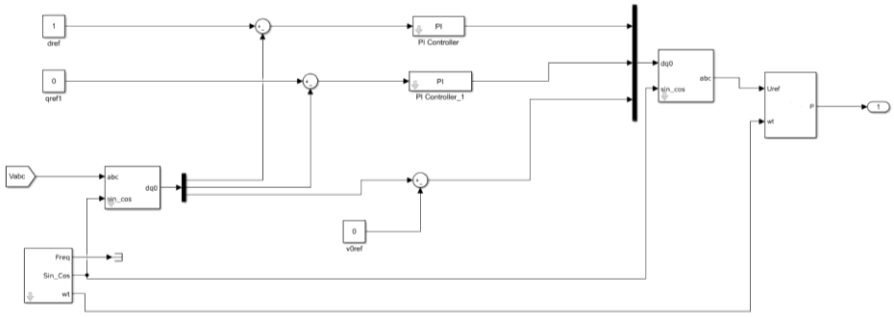

Figure 5. Proposed PI-Based control system for ZSI-DVR.

Figure 6 demonstrates the compensation performance of the proposed ZSI-DVR during a single-phase voltage sag condition. Between 0.02 s and 0.12 s, one phase of the source voltage decreases from approximately 1.0 p.u. to 0.5 p.u., corresponding to a 50% voltage sag. The ZSI-DVR injects a compensating voltage of nearly 0.5 p.u. into the affected phase through the series transformer. As observed from the load voltage waveform, the voltage remains regulated close to 1.0 p.u. throughout the disturbance interval. The compensation response is smooth and stable, indicating effective operation of the PI-controlled Z-source inverter in restoring the load voltage.

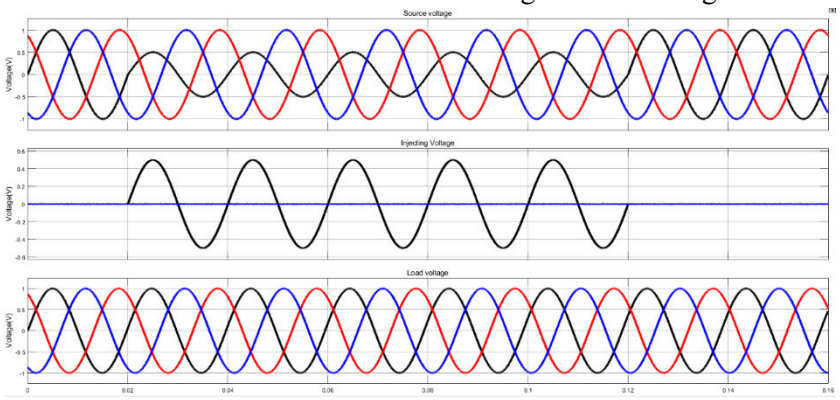

Figure 6. Single-Phase voltage sag mitigation using proposed ZSI-DVR.

Figure 7 shows the performance of the proposed ZSI-DVR under balanced three-phase voltage sag conditions. The source voltage of all three phases drops from 1.0 p.u. to approximately 0.8 p.u. during the interval from 0.02 s to 0.12 s, representing a 20% voltage sag. The DVR generates a balanced compensating voltage of approximately 0.2 p.u. per phase. Consequently, the load voltage

remains nearly constant at 1.0 p.u. throughout the disturbance period. The results verify the capability of the proposed system to provide accurate compensation during symmetrical voltage sag events.

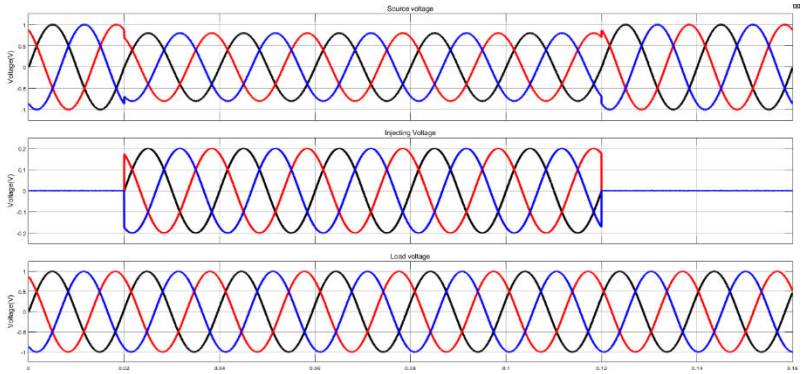

Figure 7. Balanced Three-Phase voltage sag mitigation using proposed ZSI-DVR.

Figure 8 illustrates the compensation of a severe balanced voltage sag condition using the proposed ZSI-DVR. During the disturbance interval, the source voltage magnitude decreases from approximately 1.0 p.u. to 0.5 p.u., representing a 50% sag. The Z-source inverter generates a compensating voltage close to 0.5 p.u. in each phase and injects it through the series transformer. Despite the severe reduction in source voltage, the load voltage remains maintained near the rated value of 1.0 p.u. with minimal distortion. This result demonstrates the superior voltage boosting capability provided by the Z-source network.

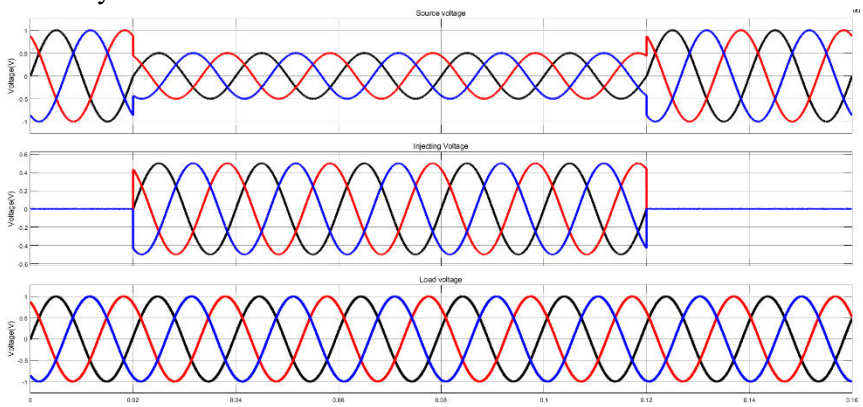

Figure 8. Severe balanced voltage sag compensation using proposed ZSI-DVR.

Figure 9 presents the harmonic analysis of the compensated load voltage under balanced voltage sag conditions. The FFT spectrum indicates a fundamental component of 50 Hz with a magnitude of approximately 0.9951 p.u. The measured Total Harmonic Distortion (THD) is only 1.94%, which is significantly lower than the 3.70% THD obtained using the conventional DVR. The harmonic spectrum shows substantial suppression of lower-order harmonic components, confirming the improved waveform quality and enhanced filtering performance of the proposed ZSI-DVR. Figure 10 illustrates the compensation capability of the proposed ZSI-DVR under unbalanced voltage sag conditions. One phase experiences a deeper sag of approximately 50%, while the remaining phases undergo moderate voltage reduction between 0.02 s and 0.12 s. The DVR generates unequal compensation voltages depending on the severity of the disturbance in each phase. The maximum injected voltage reaches approximately 0.5 p.u. in the most affected phase. After compensation, the load voltage remains balanced and maintained close to 1.0 p.u. across all phases, demonstrating the effectiveness of the proposed system in mitigating asymmetrical voltage disturbances. Figure 11 presents the FFT analysis of the load voltage after compensation of unbalanced voltage sag using the proposed ZSI-DVR. The fundamental voltage magnitude is approximately 0.9944 p.u. at the rated frequency of 50 Hz. The obtained THD is 2.44%, which is considerably lower than the 3.94% THD achieved by the conventional DVR under the same operating condition. The reduced harmonic

content indicates improved compensation accuracy and enhanced power quality performance. These results demonstrate that the proposed ZSI-DVR provides superior harmonic suppression and voltage restoration capability during unbalanced voltage sag events.

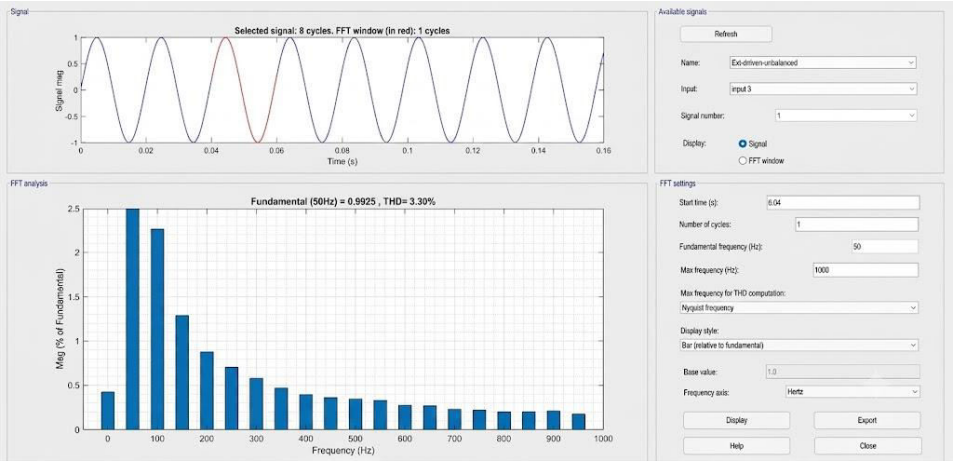

Figure 9. FFT analysis of load voltage under balanced voltage sag condition.

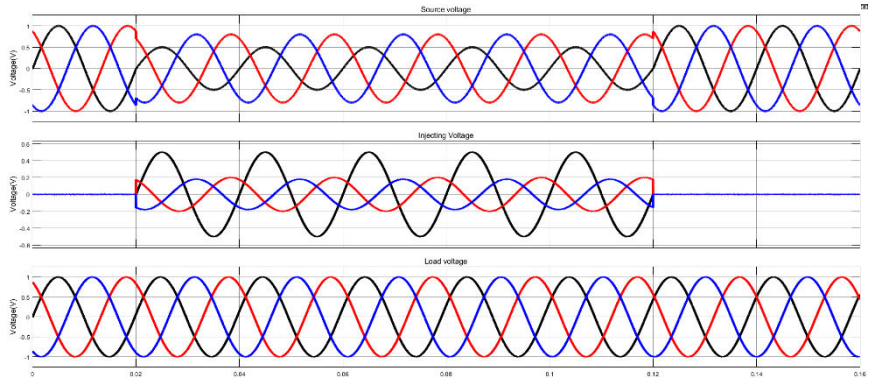

Figure 10. Unbalanced voltage sag mitigation using proposed ZSI-DVR.

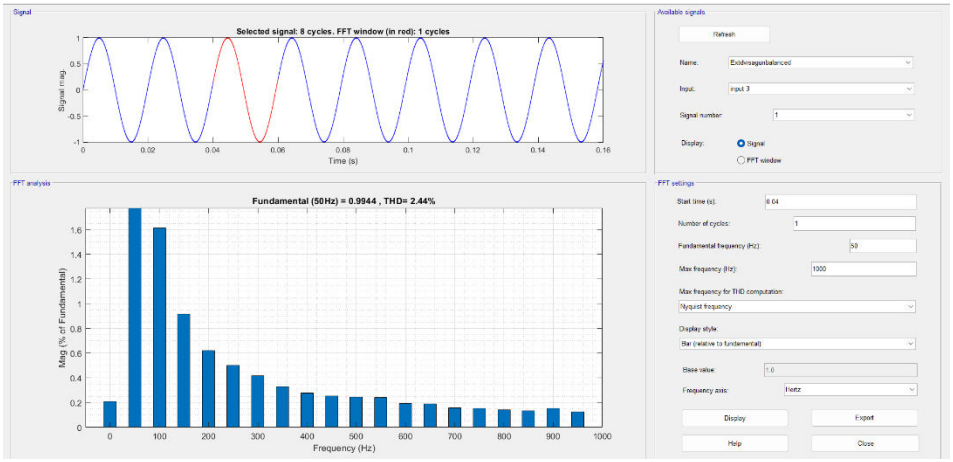

Figure 11. FFT Analysis of load voltage under unbalanced voltage sag condition.

Figure 12 illustrates the performance of the proposed ZSI-DVR under simultaneous single-phase outage and unbalanced voltage sag conditions. Between 0.02 s and 0.12 s, one phase undergoes a complete outage, resulting in a voltage magnitude of nearly 0 p.u., while the remaining phases experience voltage reduction to approximately 0.5 p.u. The ZSI-DVR generates compensating voltages reaching nearly ±1.0 p.u. for the interrupted phase and approximately ±0.5 p.u. for the sagged phases. Owing to the voltage boosting capability of the Z-source network and the precise regulation provided by the PI controller, the load voltage remains balanced and maintained close to

1.0 p.u. throughout the disturbance interval. The results confirm the capability of the proposed system to compensate severe asymmetrical disturbances without affecting load performance.

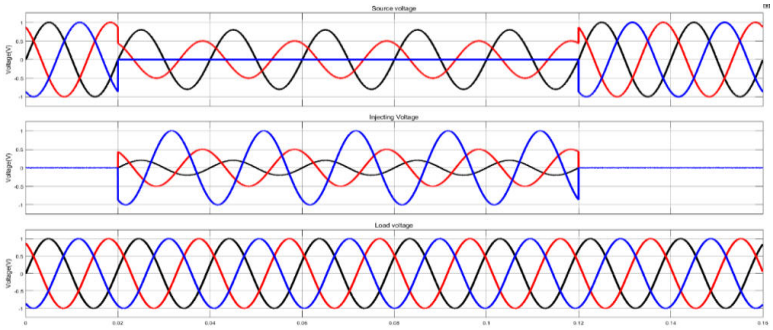

Figure 12. Single-Phase outage and unbalanced voltage sag mitigation using Proposed ZSI-DVR.

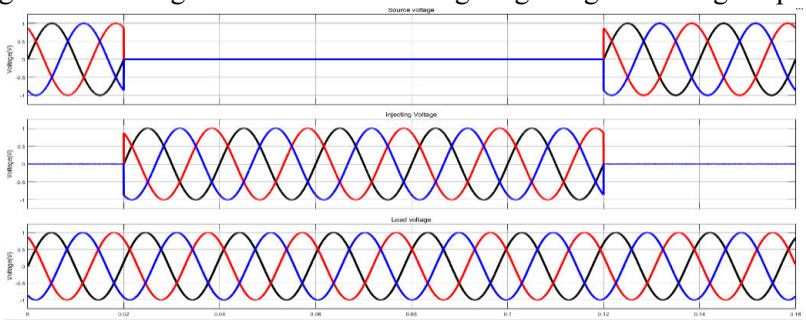

Figure 13. Three-Phase outage mitigation using proposed ZSI-DVR.

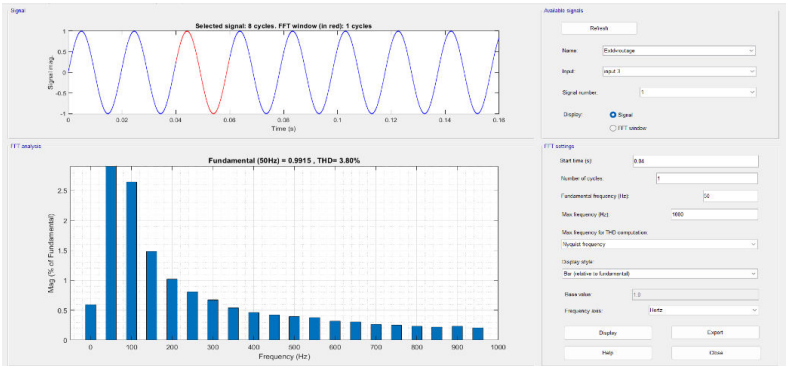

Figure 14. FFT analysis of load voltage under three-phase outage condition.

Figure 13 presents the response of the proposed ZSI-DVR during a complete three-phase outage condition. At approximately 0.02 s, all three source voltages collapse to 0 p.u. and remain interrupted until 0.12 s, representing a 100% three-phase outage. During this interval, the ZSI-DVR injects the full compensation voltage of approximately ±1.0 p.u. into all three phases using the stored DC-link energy and Z-source boosting mechanism. As observed in the load voltage waveform, the rated voltage of approximately 1.0 p.u. is continuously maintained throughout the outage period. This demonstrates the superior voltage support capability of the proposed system during complete supply interruptions. Figure 14 shows the FFT analysis of the compensated load voltage under the three-phase outage condition. The fundamental frequency component is maintained at 50 Hz with a magnitude of approximately 0.9915p.u. The measured Total Harmonic Distortion (THD) is 3.80%, which is lower than the 4.57% obtained using the conventional DVR. The harmonic spectrum indicates significant attenuation of lower-order harmonics and improved waveform quality. The reduced THD value confirms the effectiveness of the Z-source network and PI-controlled compensation strategy in maintaining superior power quality during complete voltage interruption events. Figure 15 illustrates the compensation performance of the proposed ZSI-DVR during a balanced three-phase voltage swell condition. Between 0.02 s and 0.12 s, the source voltage magnitude increases from approximately 1.0p.u. to nearly 2.0p.u., representing a 100% voltage

swell. To counteract the excessive voltage, the DVR injects an opposing compensating voltage of approximately −1.0p.u. in each phase. As a result, the load voltage remains regulated at approximately 1.0p.u. throughout the disturbance interval. The smooth compensation waveform demonstrates the capability of the ZSI-DVR to effectively suppress severe overvoltage conditions while maintaining excellent voltage quality.

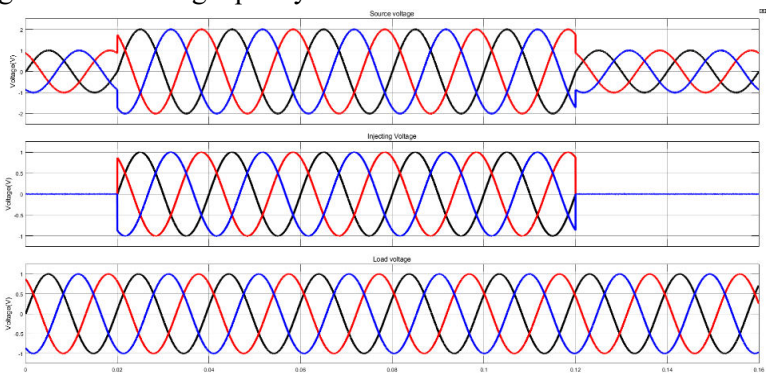

Figure 15. Balanced voltage swell mitigation using proposed ZSI-DVR.

Figure 16 presents the harmonic analysis of the load voltage after compensation of balanced voltage swell. The FFT spectrum shows a fundamental component of 50 Hz with a magnitude of approximately 0.9926p.u. The Total Harmonic Distortion is measured as 3.02%, which is significantly lower than the 4.10% obtained using the existing DVR. The harmonic components beyond the fundamental frequency are considerably reduced, demonstrating enhanced waveform quality. The results indicate that the proposed ZSI-DVR effectively maintains power quality while compensating severe balanced voltage swell disturbances.

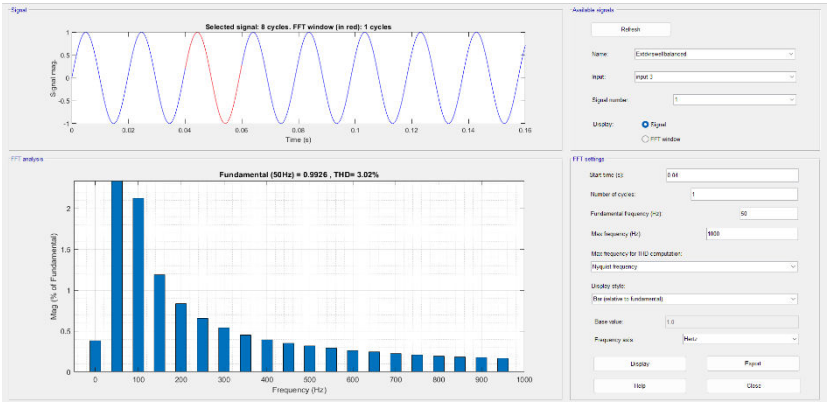

Figure 16. FFT analysis of load voltage under balanced voltage swell condition.

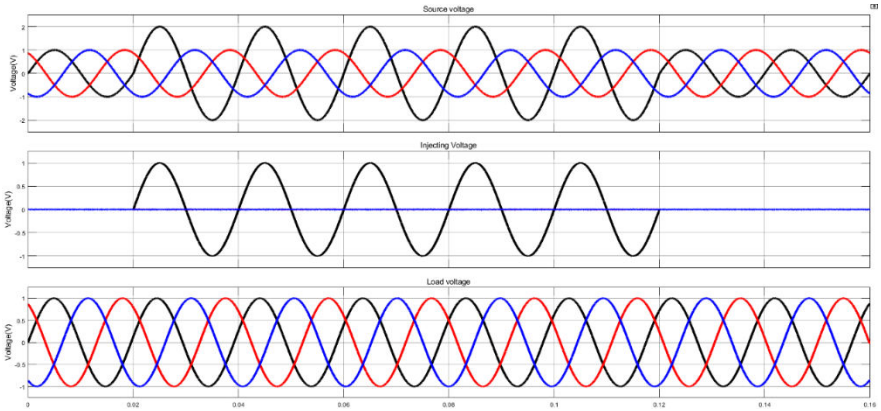

Figure 17. Single-Phase voltage swell mitigation using proposed ZSI-DVR.

Figure 17 shows the operation of the proposed ZSI-DVR during a single-phase voltage swell condition. One phase experiences a voltage increases from approximately 1.0p.u. to nearly 2.0p.u.

between 0.02 s and 0.12 s, while the remaining phases remain unaffected. To compensate for the overvoltage, the DVR injects a counteracting voltage of approximately −1.0p.u. into the affected phase. Consequently, the load voltage remains balanced and regulated close to the rated value of 1.0p.u. throughout the disturbance period. The result demonstrates the capability of the proposed ZSI-DVR to effectively suppress asymmetrical overvoltage disturbances. Figure 18 illustrates the compensation performance of the proposed ZSI-DVR under unbalanced voltage swell conditions. During the disturbance interval, different phases experience unequal voltage increases, with the highest swell magnitude approaching 2.0p.u. The DVR generates phase-specific compensating voltages ranging between approximately −0.5p.u. and −1.0p.u. depending on the severity of the disturbance. After compensation, all three load voltages remain balanced and close to 1.0p.u. The figure demonstrates the ability of the proposed system to mitigate severe asymmetrical voltage swell conditions while maintaining stable operation and high-quality load voltage.

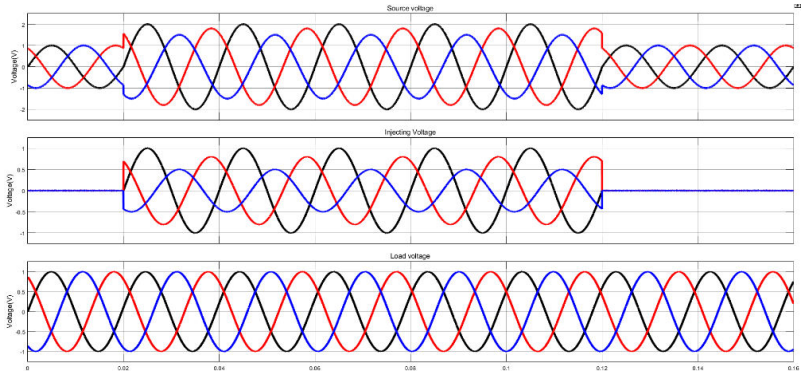

Figure 18. Unbalanced voltage swell mitigation using proposed ZSI-DVR

Figure 19 presents the FFT analysis of the compensated load voltage during unbalanced voltage swell mitigation. The fundamental voltage component is maintained at 50 Hz with a magnitude of approximately 0.9925p.u. The measured Total Harmonic Distortion is 3.30%, which is considerably lower than the 4.52% THD obtained using the conventional DVR. The harmonic spectrum indicates effective suppression of lower-order and higher-order harmonic components. The reduced THD and improved fundamental voltage magnitude confirm the superior compensation capability and enhanced power quality performance of the proposed ZSI-DVR under unbalanced voltage swell conditions.

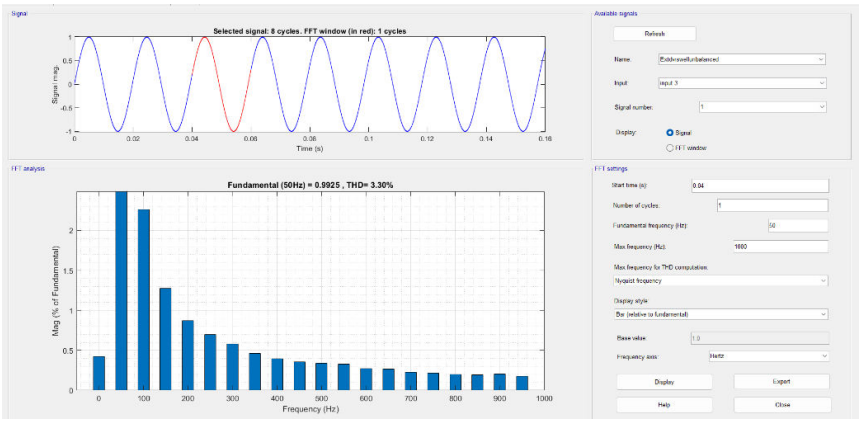

Figure 19. FFT analysis of load voltage under unbalanced voltage swell condition.

Table 2 compares the harmonic performance of the existing DVR and the proposed ZSI-DVR under voltage sag and outage conditions. The proposed ZSI-DVR consistently achieves lower Total Harmonic Distortion values in all operating scenarios. Under balanced voltage sag, THD is reduced from 3.70% to 1.94%, representing a significant improvement in waveform quality. Similarly, under unbalanced voltage sag, THD decreases from 3.94% to 2.44%. During the severe three-phase outage

condition, the proposed system maintains THD at 3.80%, compared to 4.57% in the conventional DVR. These results demonstrate the superior filtering capability and compensation accuracy of the Z-source inverter topology.

Table 2. Comparison of THD performance under voltage sag conditions.

Operating Condition	Existing DVR THD (%)	Proposed ZSI-DVR THD (%)
Balanced Voltage Sag	3.70	1.94
Unbalanced Voltage Sag	3.94	2.44
Three-Phase Outage	4.57	3.80

Table 3 presents the harmonic distortion comparison during voltage swell compensation. The proposed ZSI-DVR achieves noticeable harmonic reduction in both balanced and unbalanced swell conditions. For balanced voltage swell, THD decreases from 4.10% to 3.02%, while under unbalanced voltage swell, THD reduces from 4.52% to 3.30%. The lower distortion levels indicate that the PI-controlled Z-source inverter produces smoother compensation voltages and improves the quality of the load voltage supplied to sensitive equipment.

Table 3. Comparison of THD performance under voltage swell conditions.

Operating Condition	Existing DVR THD (%)	Proposed ZSI-DVR THD (%)
Balanced Voltage Swell	4.10	3.02
Unbalanced Voltage Swell	4.52	3.30

Table 4 compares the fundamental load voltage magnitudes achieved after compensation. The proposed ZSI-DVR maintains the load voltage closer to the ideal rated value of 1.0 p.u. in all disturbance conditions. The improvement is particularly noticeable under balanced and unbalanced voltage sag conditions where the fundamental component reaches 0.9951 p.u. and 0.9944 p.u., respectively. These results indicate that the Z-source network and PI controller provide more accurate voltage restoration than the conventional DVR.

Table 4. Comparison of fundamental voltage magnitude.

Operating Condition	Existing DVR (p.u.)	Proposed ZSI-DVR (p.u.)
Balanced Voltage Sag	0.9914	0.9951
Unbalanced Voltage Sag	0.9918	0.9944
Three-Phase Outage	0.9909	0.9915
Balanced Voltage Swell	0.9912	0.9926
Unbalanced Voltage Swell	0.9916	0.9925

Table 5. Overall performance comparison

Parameter	Existing DVR	Proposed ZSI-DVR
Inverter Type	VSI	Z-Source Inverter
Controller	DQ0 Control	PI + DQ0 Control
Voltage Boost Capability	Limited	High
THD Reduction	Moderate	Excellent
Fundamental Voltage Accuracy	Good	Very High
Dynamic Response	Moderate	Fast
Voltage Restoration Accuracy	Good	Excellent
Harmonic Suppression	Moderate	Superior
Power Quality Improvement	Good	Excellent
System Reliability	Good	Excellent

Table 5 summarizes the overall performance comparison between the existing DVR and the proposed ZSI-DVR. The conventional DVR employs a standard VSI and basic DQ0 control strategy, whereas the proposed system utilizes a Z-source inverter integrated with a PI controller. The Z-source impedance network provides inherent voltage boosting capability, enabling improved compensation performance without requiring an additional DC–DC converter. As reflected in the THD values, voltage restoration accuracy, and power quality indices, the proposed ZSI-DVR delivers superior overall performance, enhanced reliability, faster response, and improved load voltage quality under all tested disturbance conditions.

5. Conclusion

This work successfully demonstrated the effectiveness of the proposed ZSI-DVR with PI controller for mitigating various power quality disturbances including voltage sag, voltage swell, single-phase outage, three-phase outage, and unbalanced operating conditions. Compared with the existing VSI-based DVR, the proposed ZSI-DVR exhibited superior performance in terms of voltage restoration accuracy, harmonic reduction, and overall power quality improvement. Under balanced voltage sag conditions, the proposed system reduced THD from 3.70% to 1.94%, while under unbalanced voltage sag conditions THD decreased from 3.94% to 2.44%. Similarly, during three-phase outage compensation, THD improved from 4.57% to 3.80%. For balanced and unbalanced voltage swell conditions, the proposed system achieved THD values of 3.02% and 3.30%, compared with 4.10% and 4.52% obtained using the existing DVR. The incorporation of the Z-source network provided inherent voltage boosting capability without requiring an additional DC–DC converter, enabling effective compensation of severe disturbances. Furthermore, the PI controller enhanced dynamic response, reduced steady-state error, and maintained the load voltage very close to the rated value under all operating conditions. The simulation results clearly confirm that the proposed ZSI-DVR offers improved harmonic suppression, better voltage regulation, higher compensation capability, enhanced reliability, and superior power quality performance compared to the conventional VSI-based DVR, making it a suitable solution for protecting sensitive loads in modern power distribution systems.

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